

FIG. 1A (Prior Art)

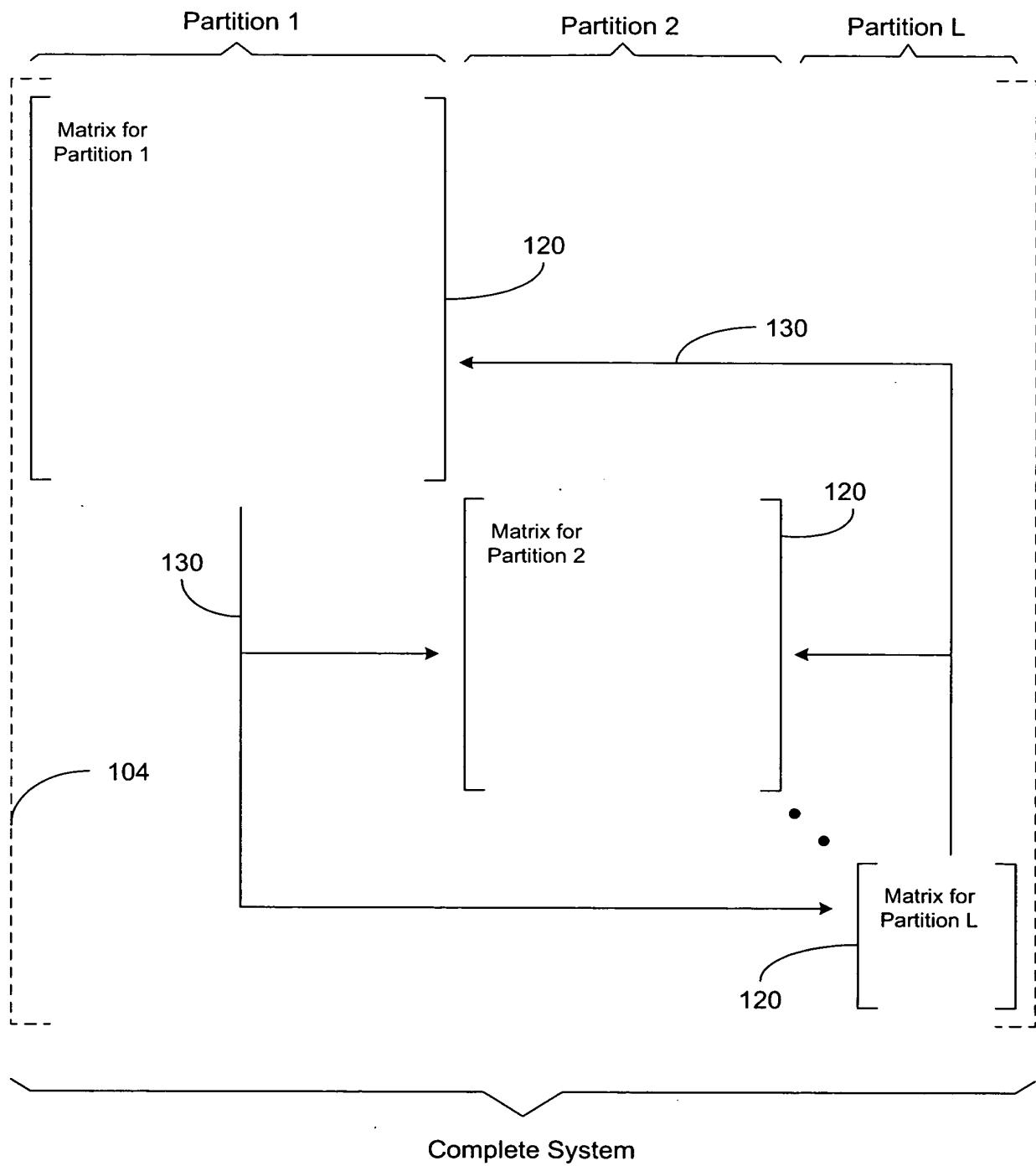


FIG. 1B (Prior Art)

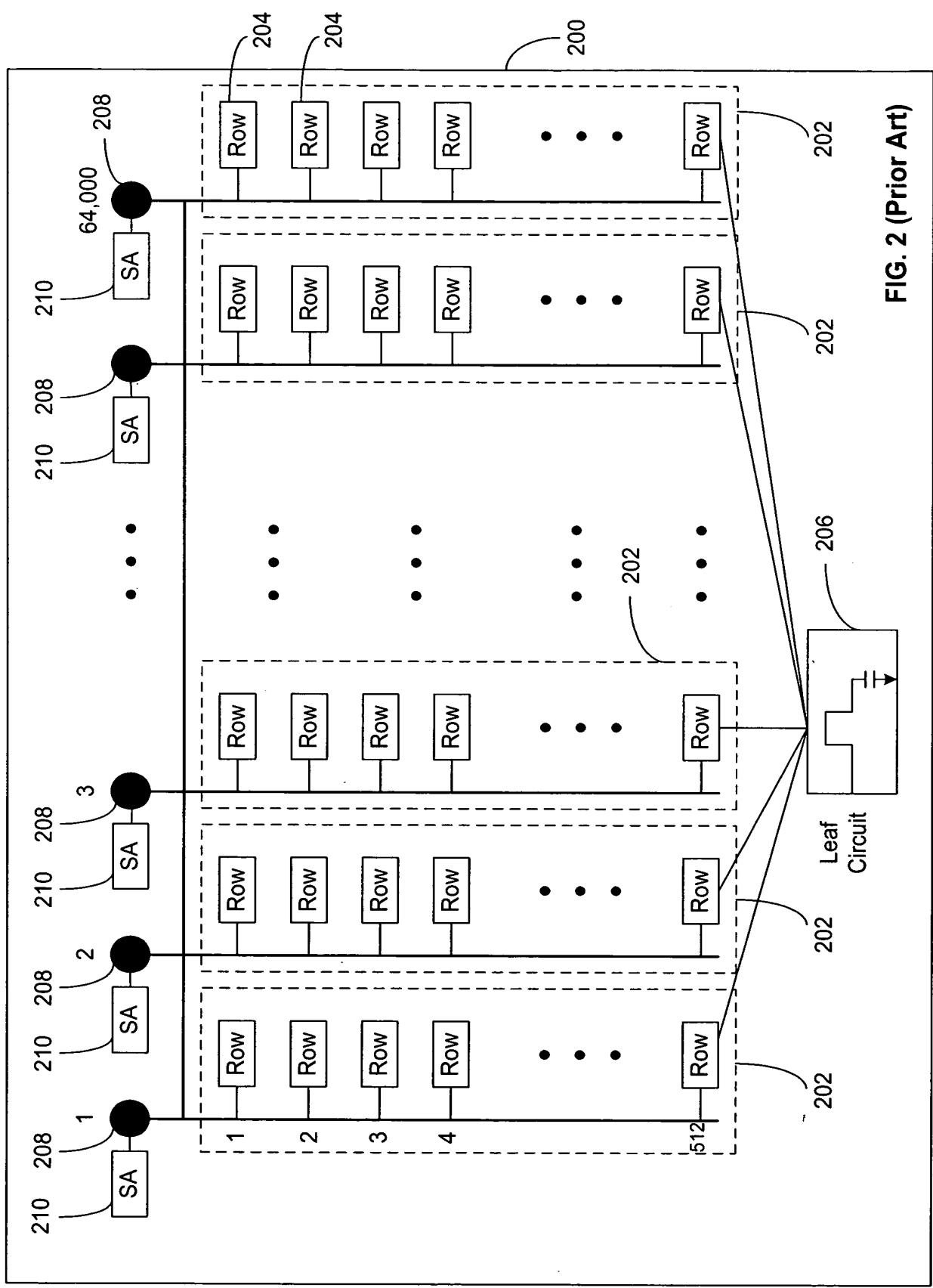
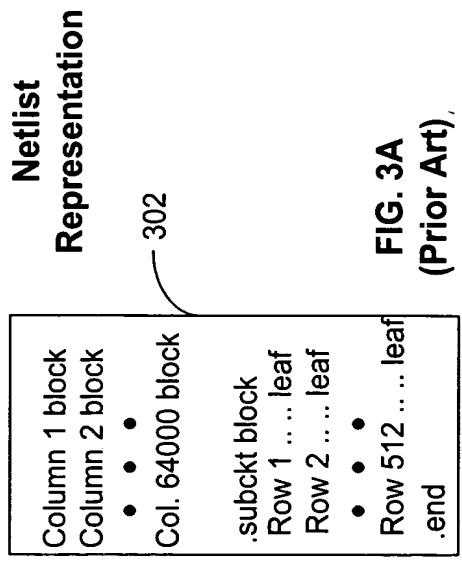


FIG. 2 (Prior Art)



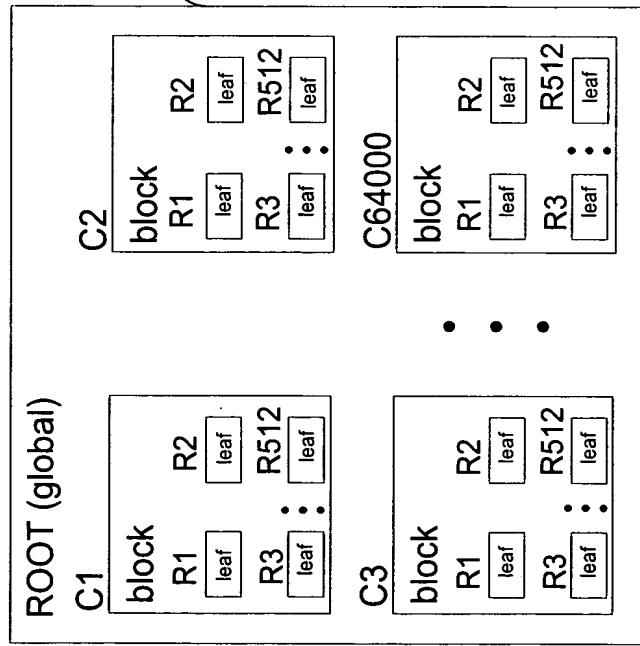
Flat Representation

C1.R1	C2.R1	C64000.R1
leaf	leaf	leaf
C1.R2	C2.R2	C64000.R2
leaf	leaf	leaf
...
C1.R512	C2.R512	C64000.R512
leaf	leaf	leaf
...

306

FIG. 3C
(Prior Art)

Physical Representation



302

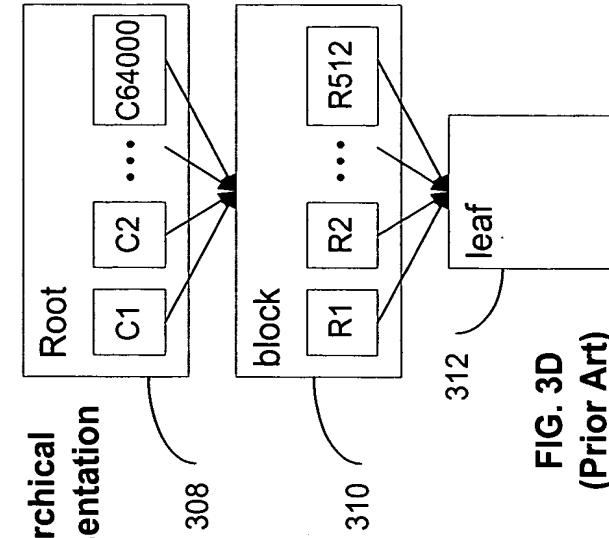
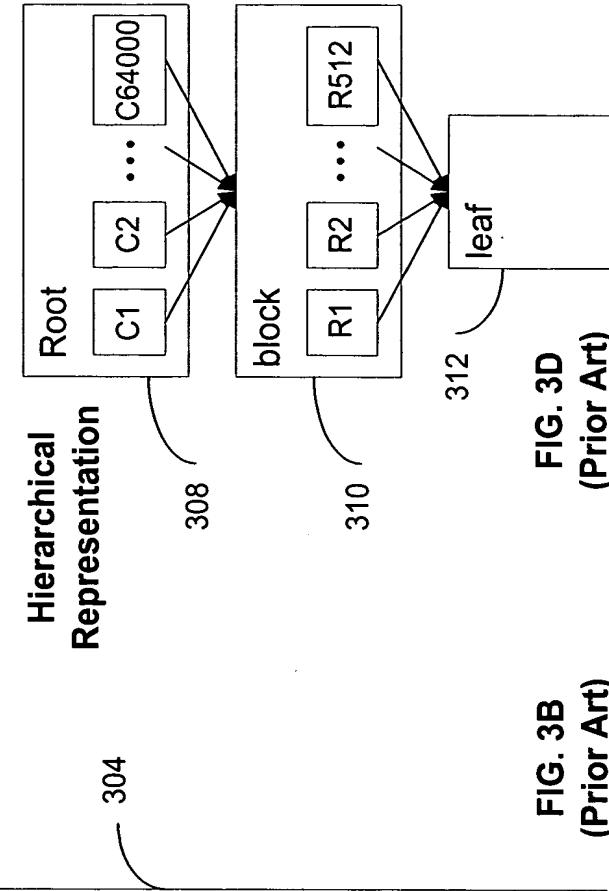
.subckt block

Row 1 ... leaf

Row 2 ... leaf

• • •

Row 512 ... leaf
.end



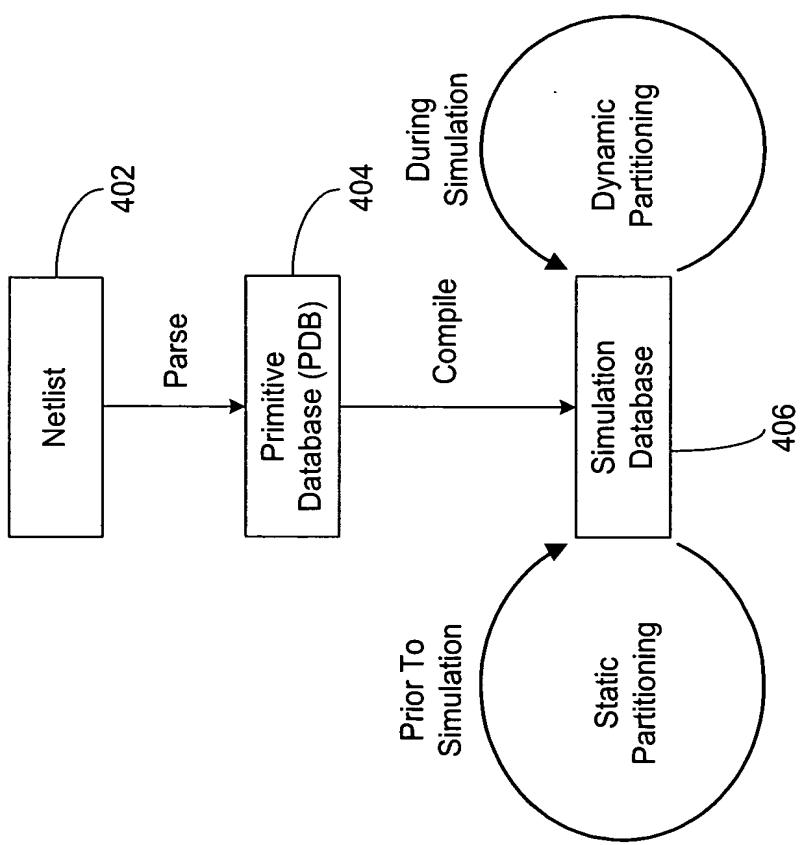


FIG. 4 (Prior Art)

Static Partitioning

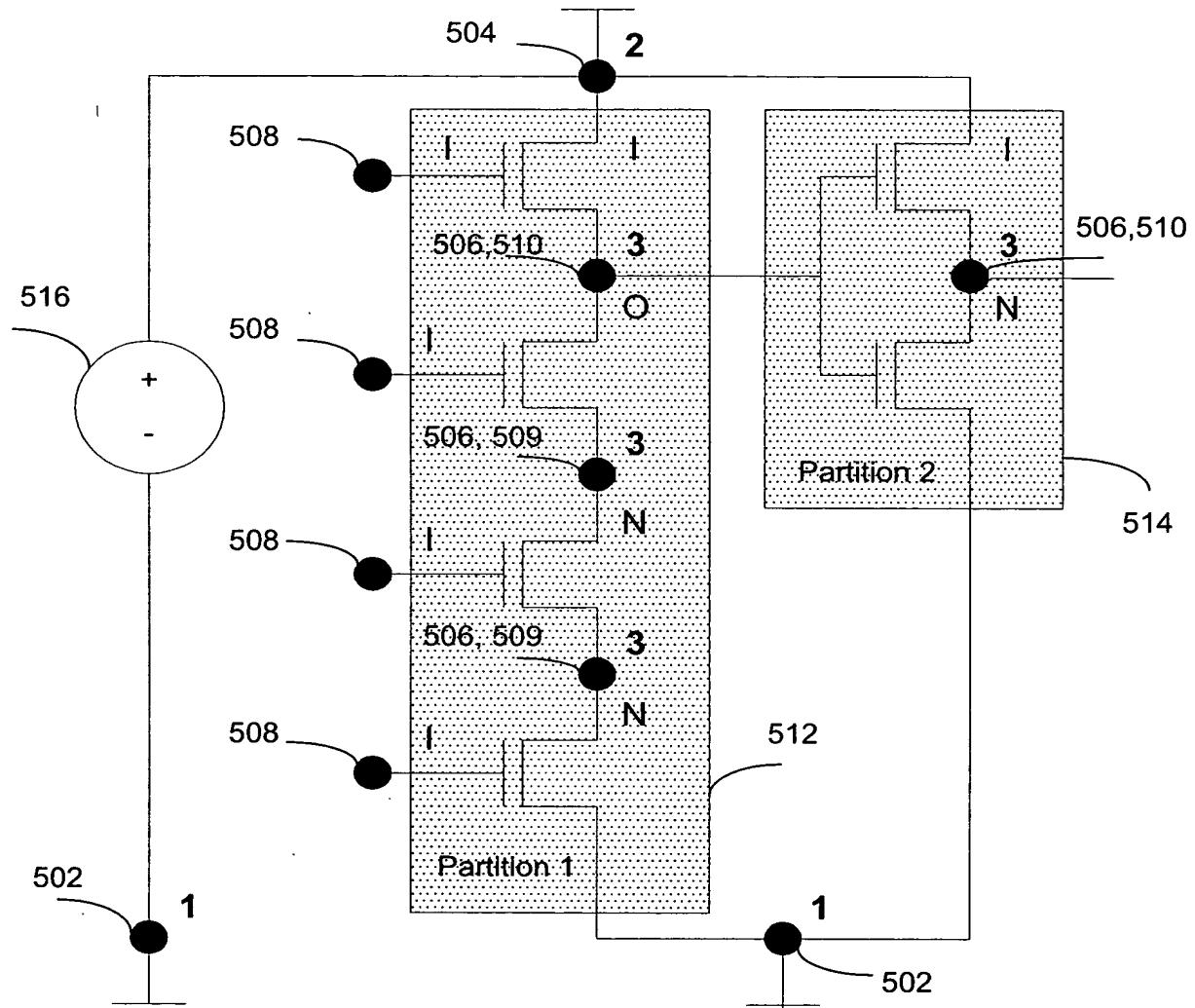


FIG. 5 (Prior Art)

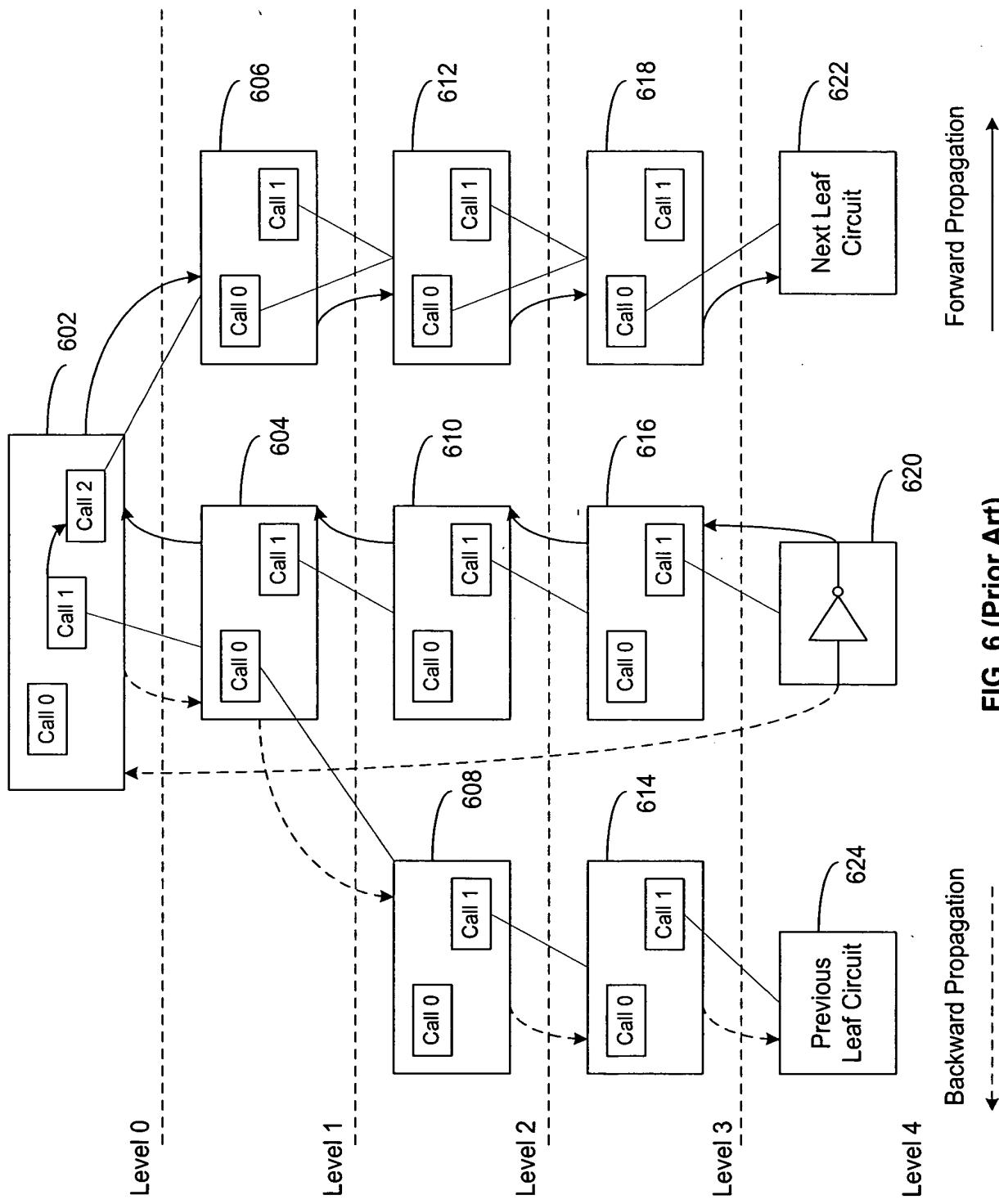


FIG. 6 (Prior Art)

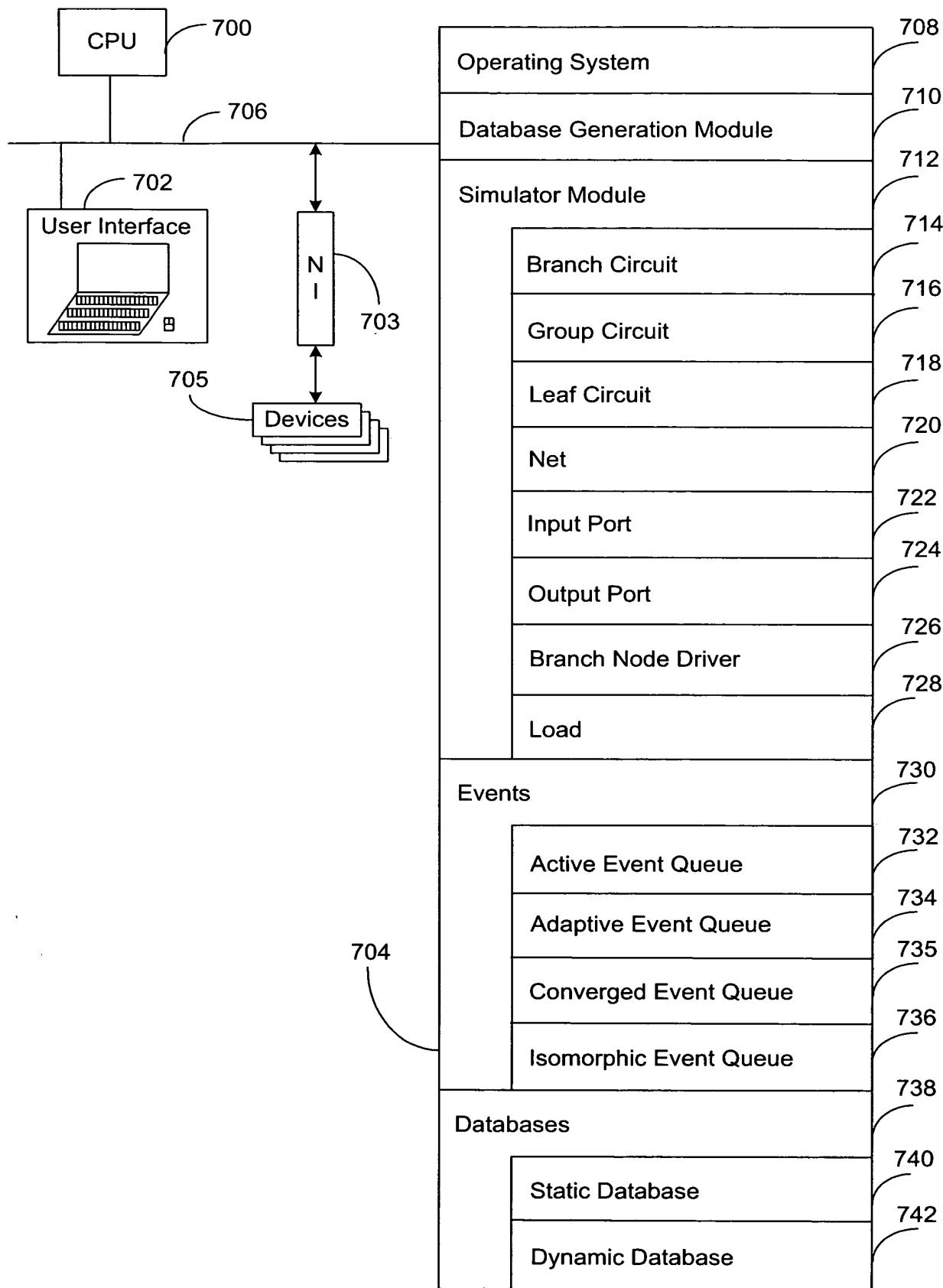


FIG. 7

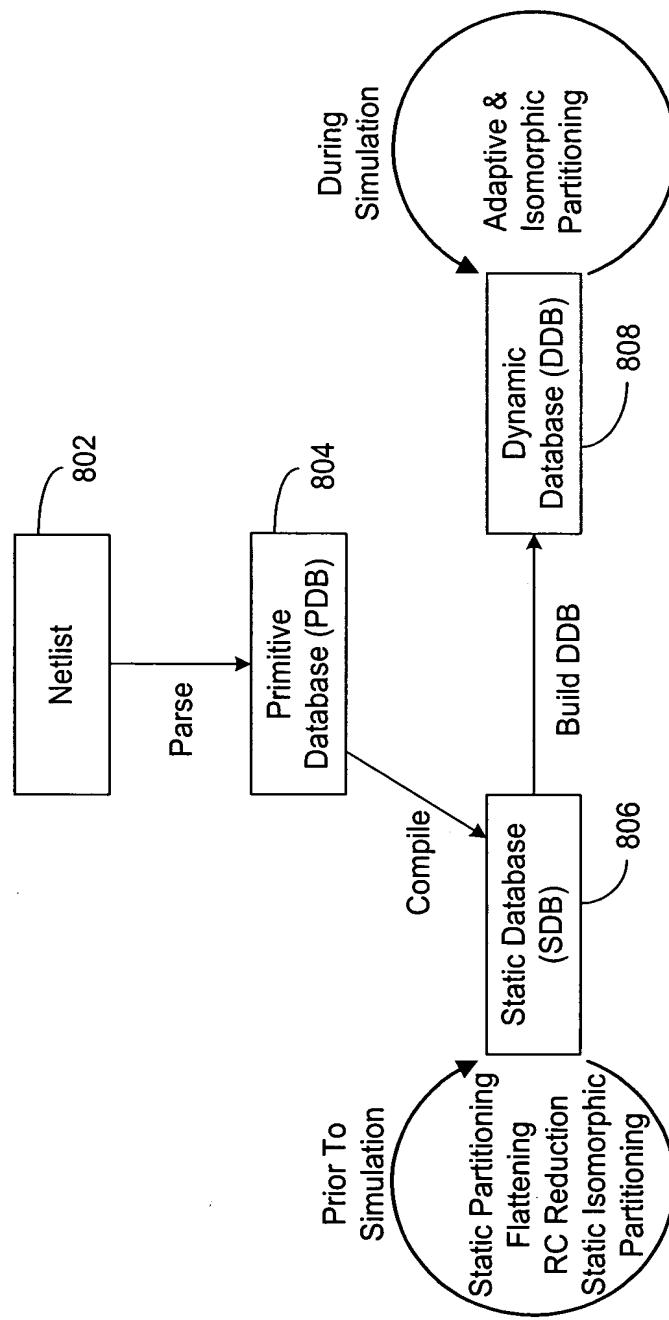


FIG. 8A

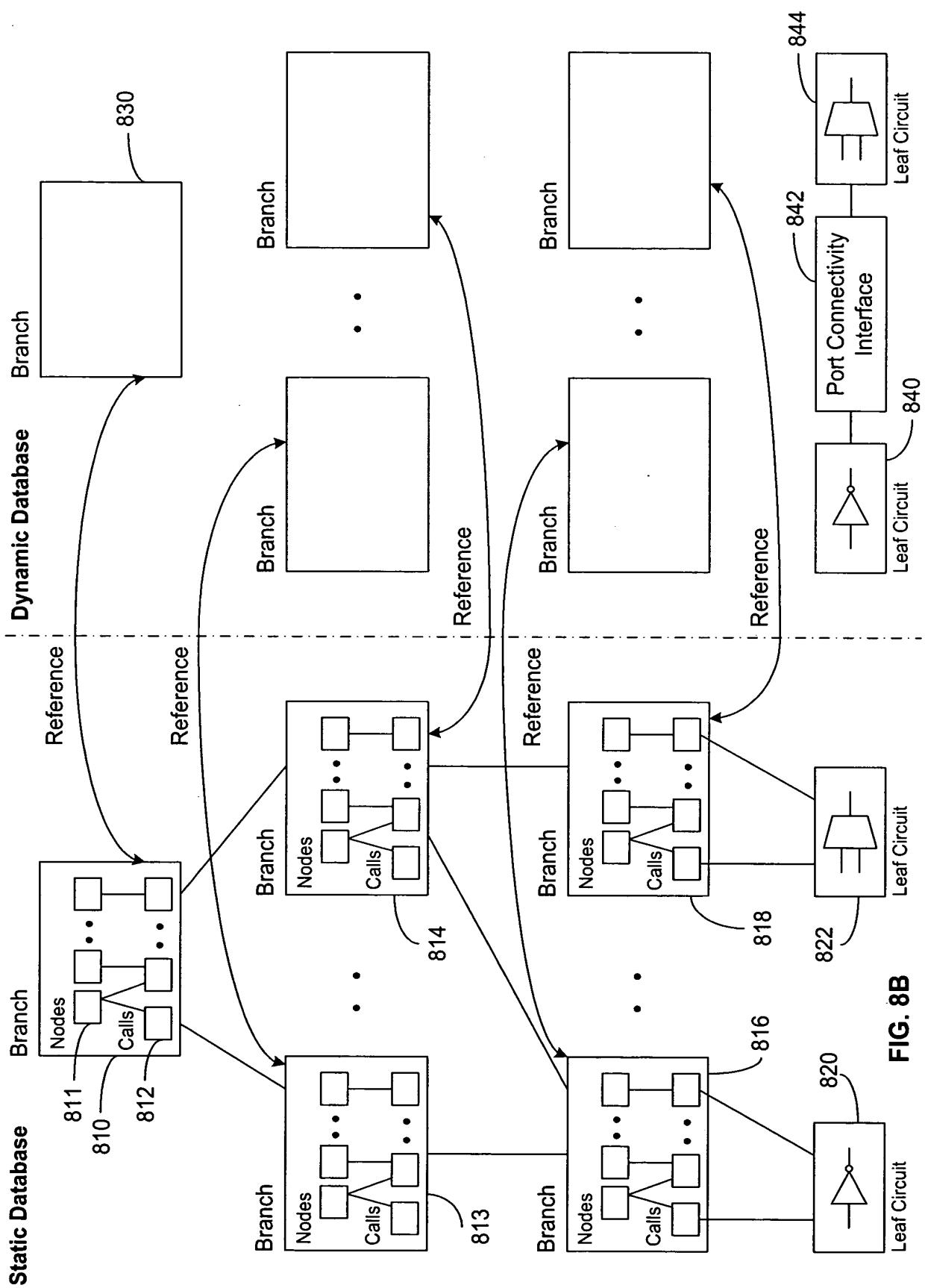


FIG. 8B

Leaf Circuit
Leaf Circuit

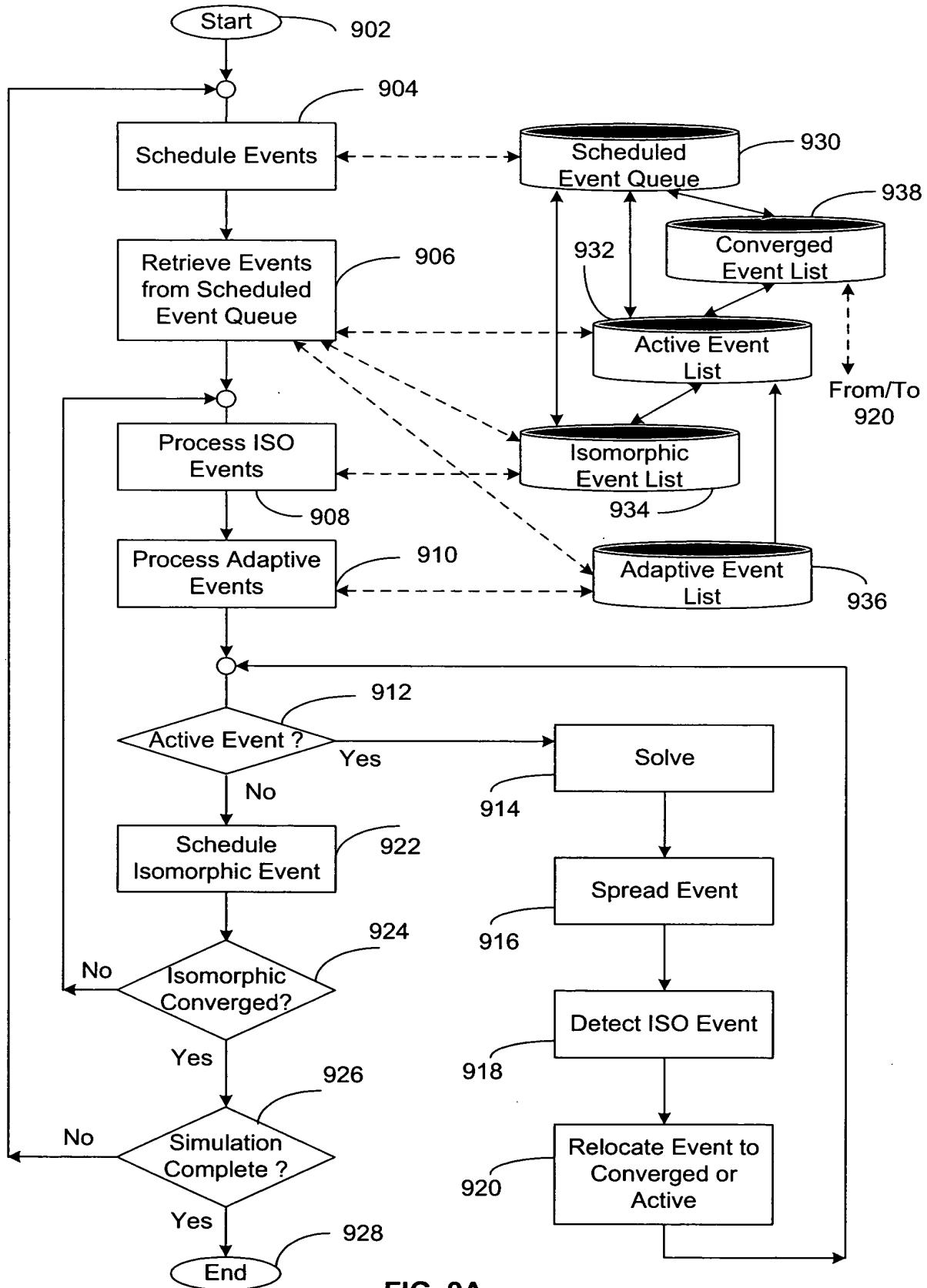


FIG. 9A

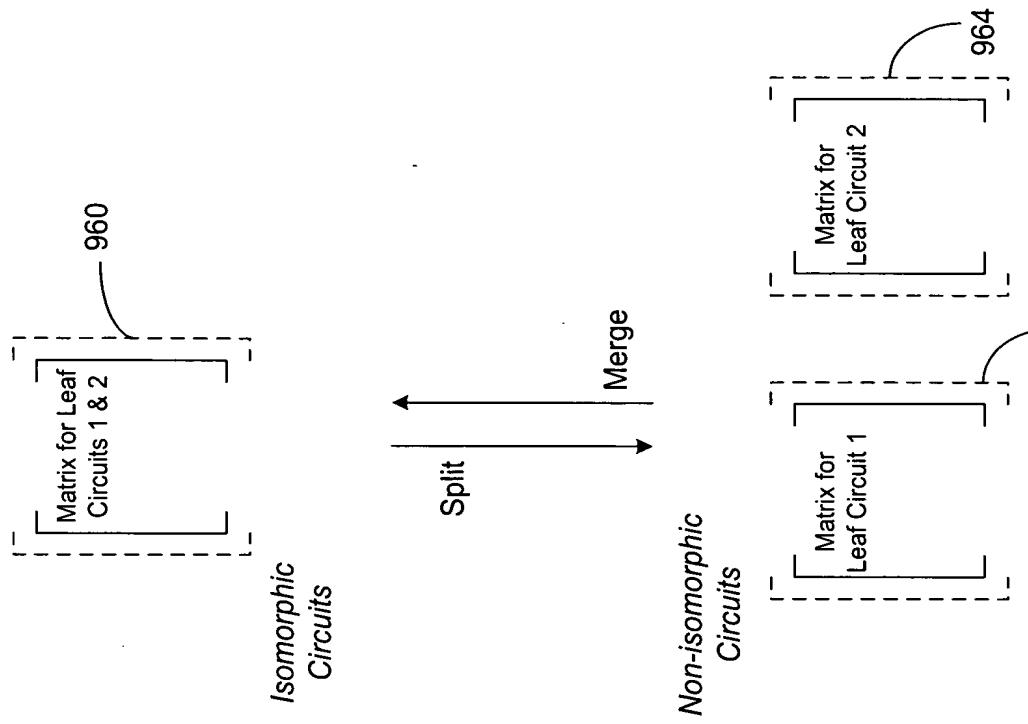
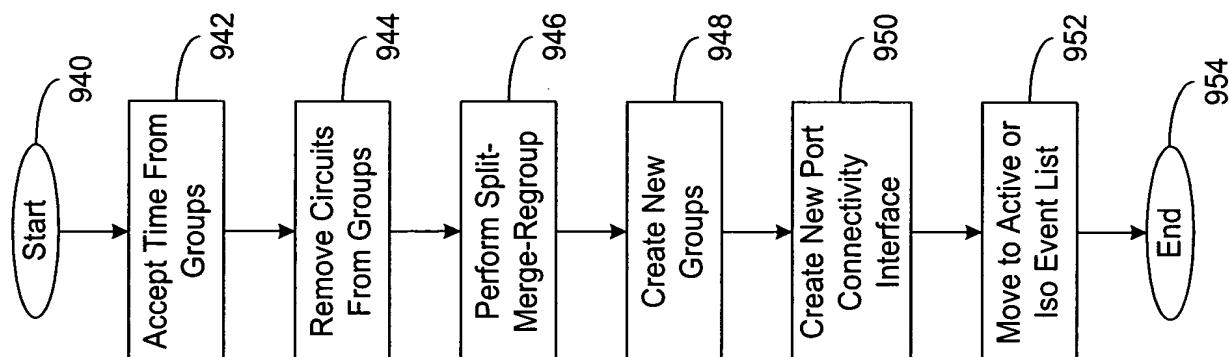


FIG. 9B

FIG. 9C

FIG. 10A

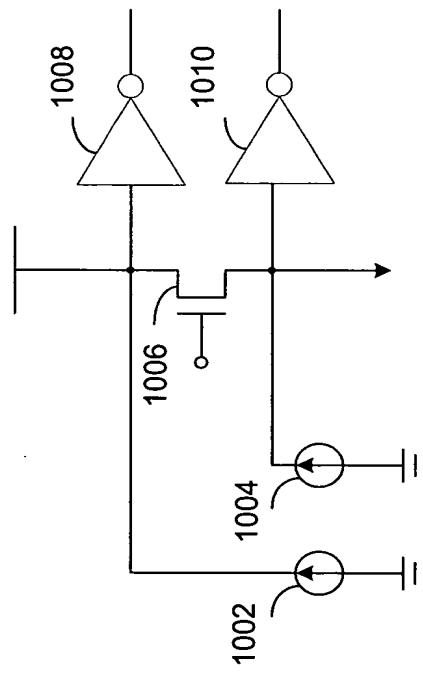
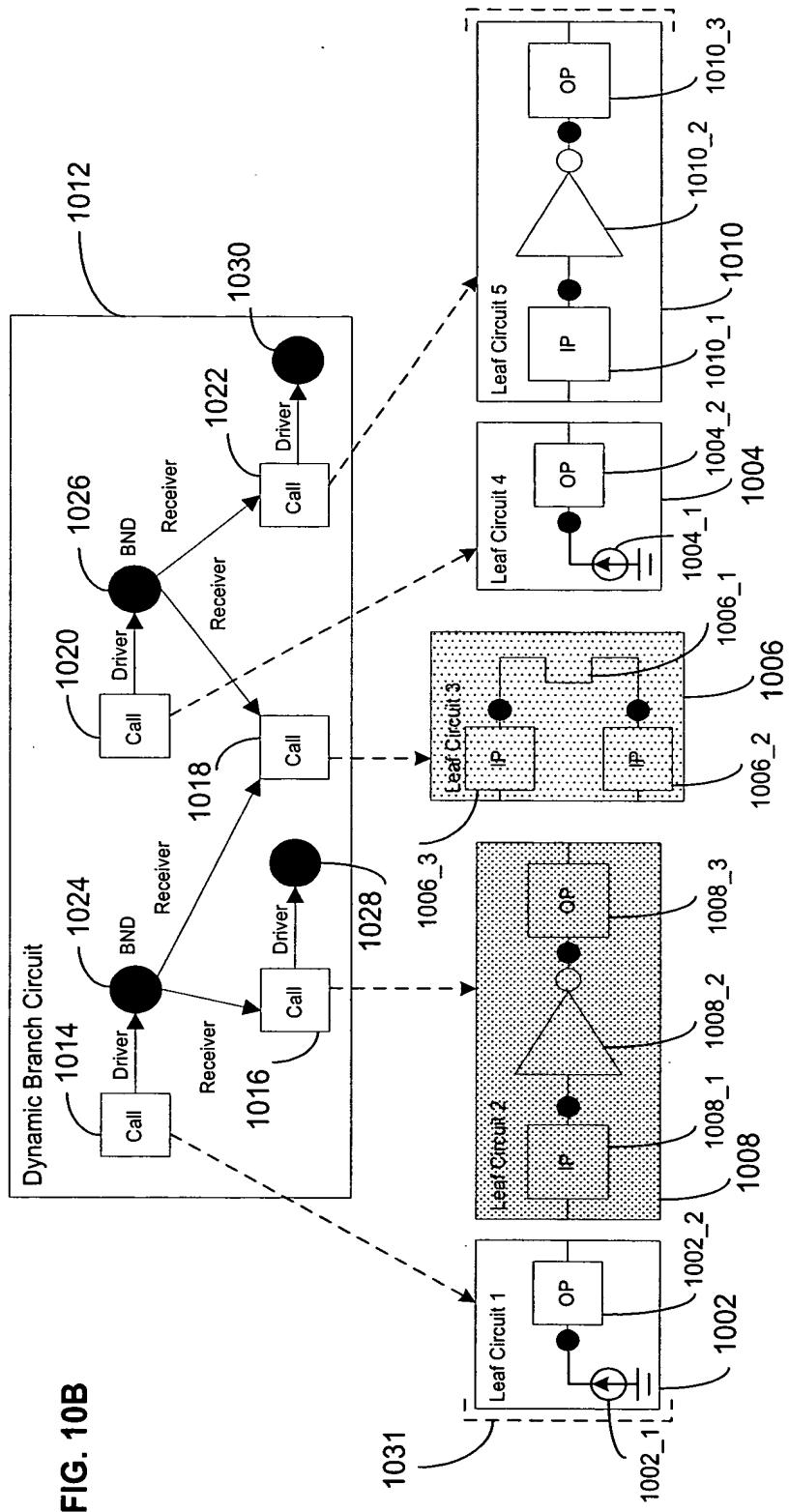


FIG. 10B



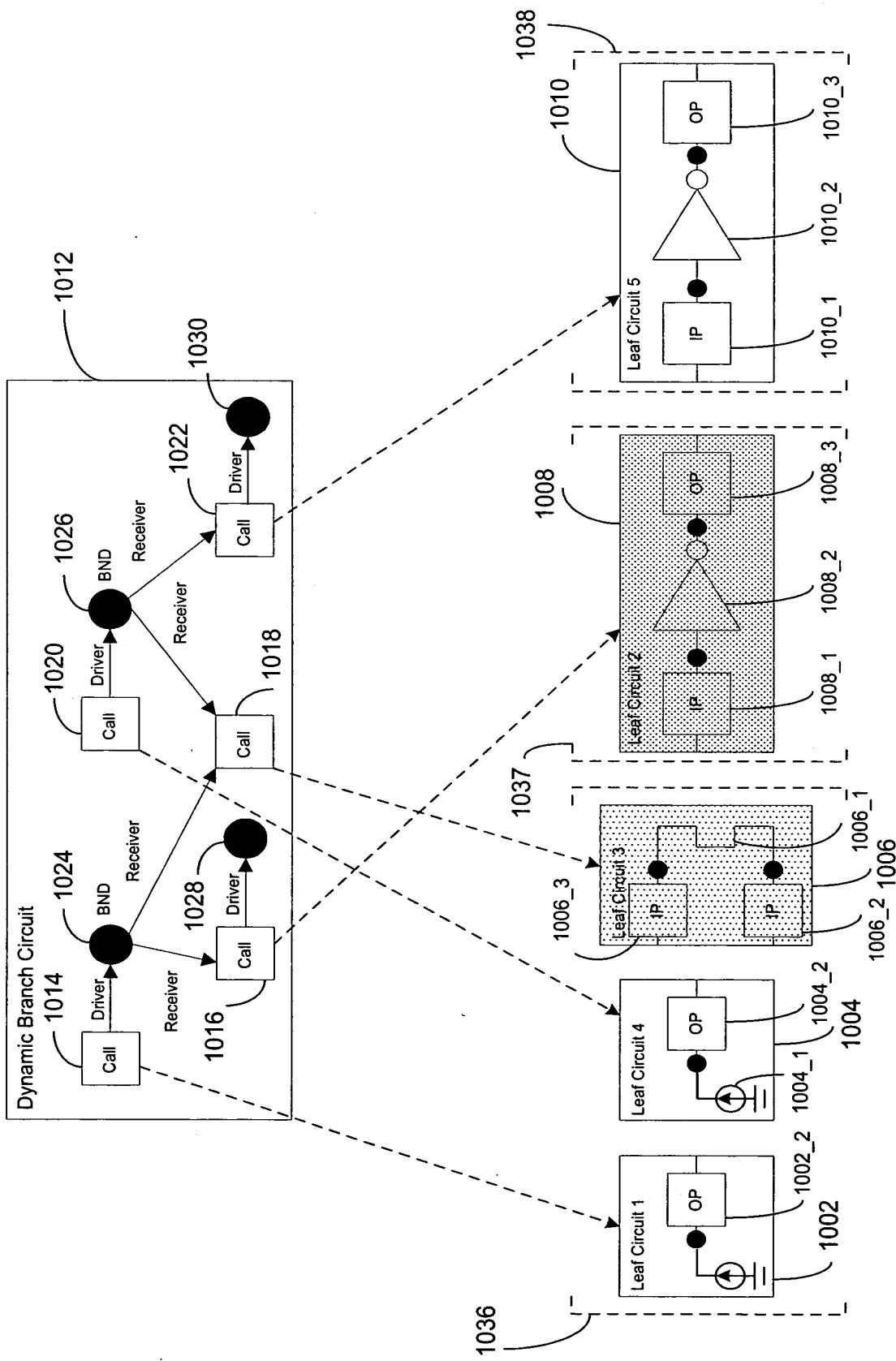


FIG. 10C

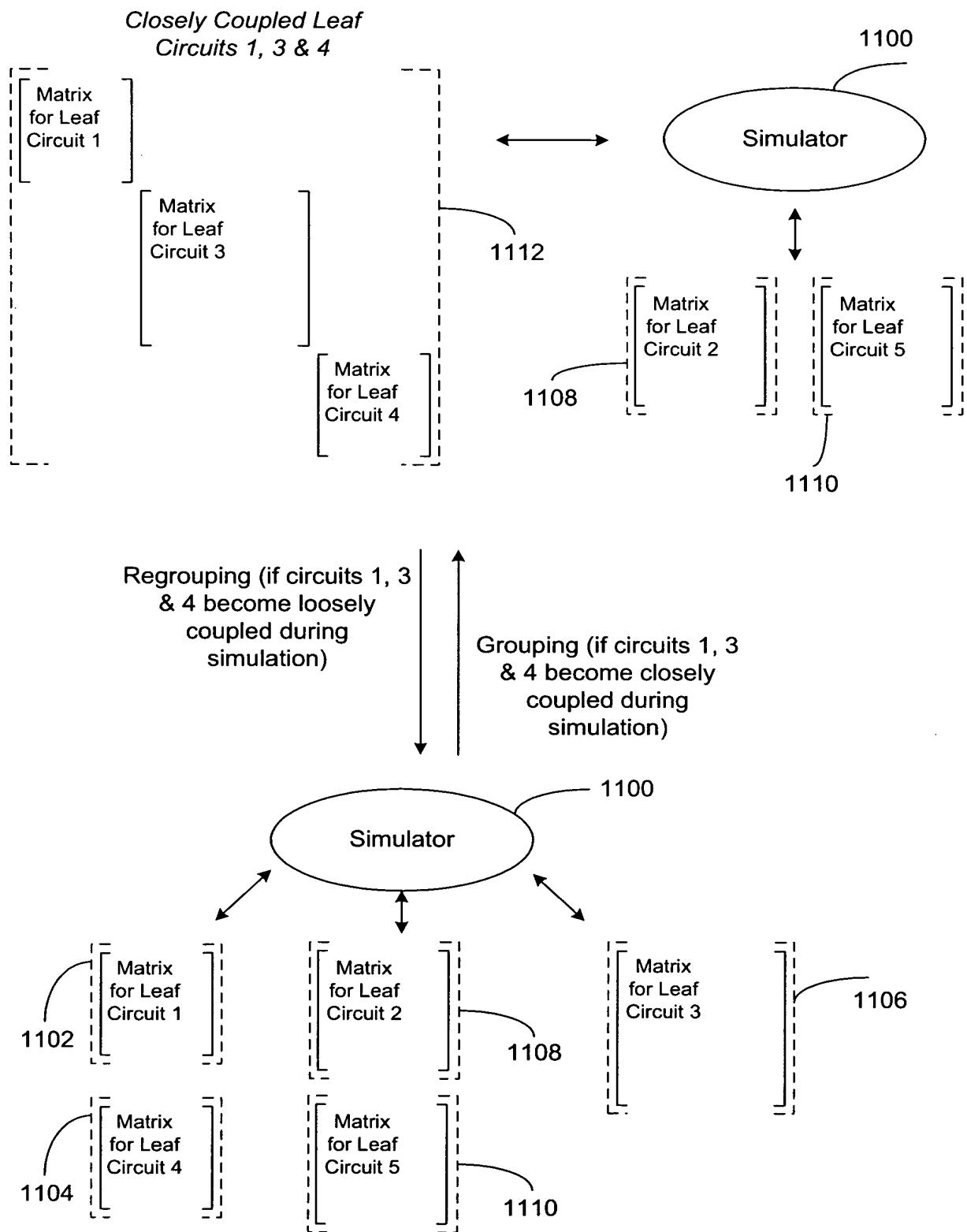


FIG. 11

Loosely Coupled Leaf Circuits

FIG. 12A

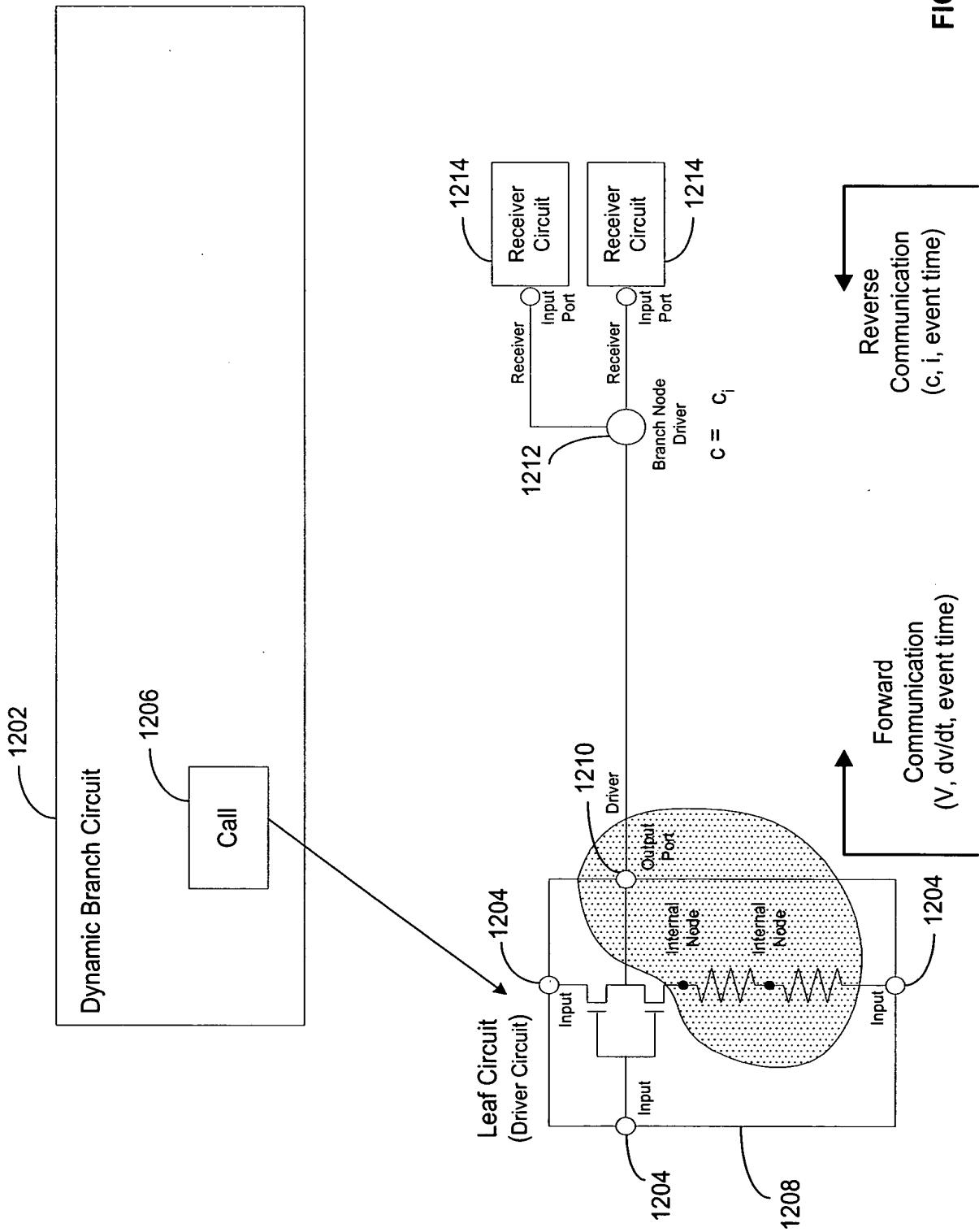
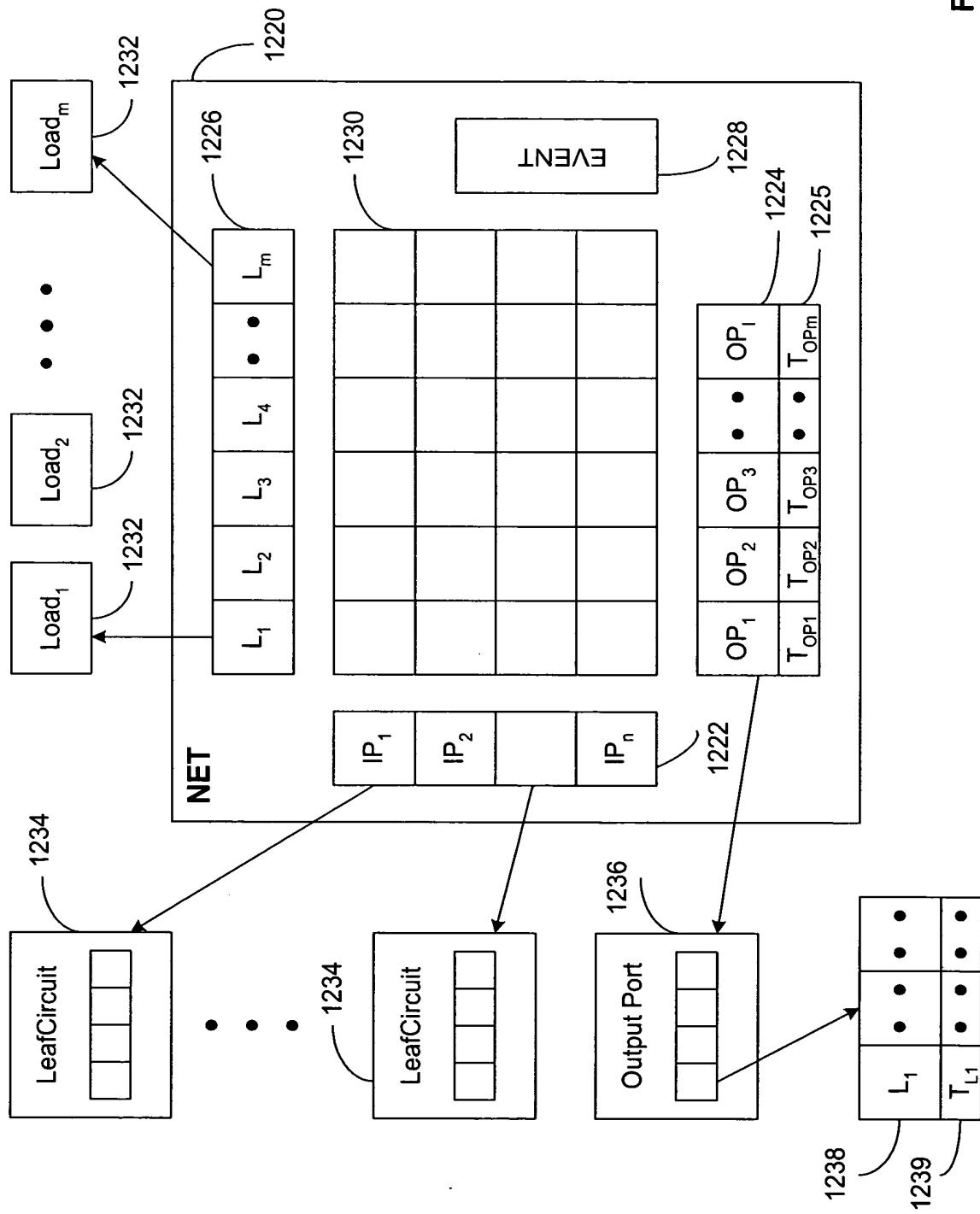


FIG. 12B



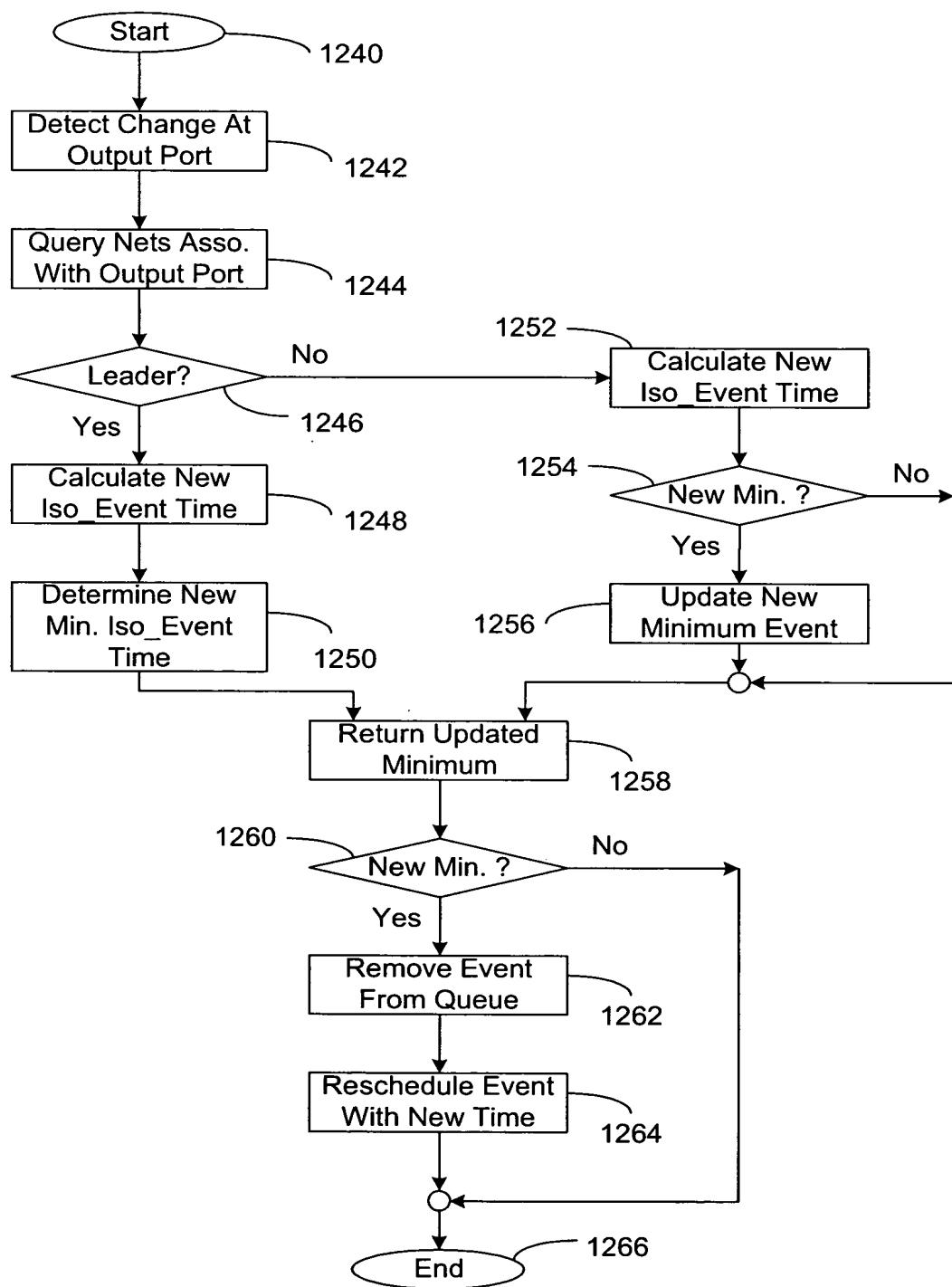


FIG. 12C

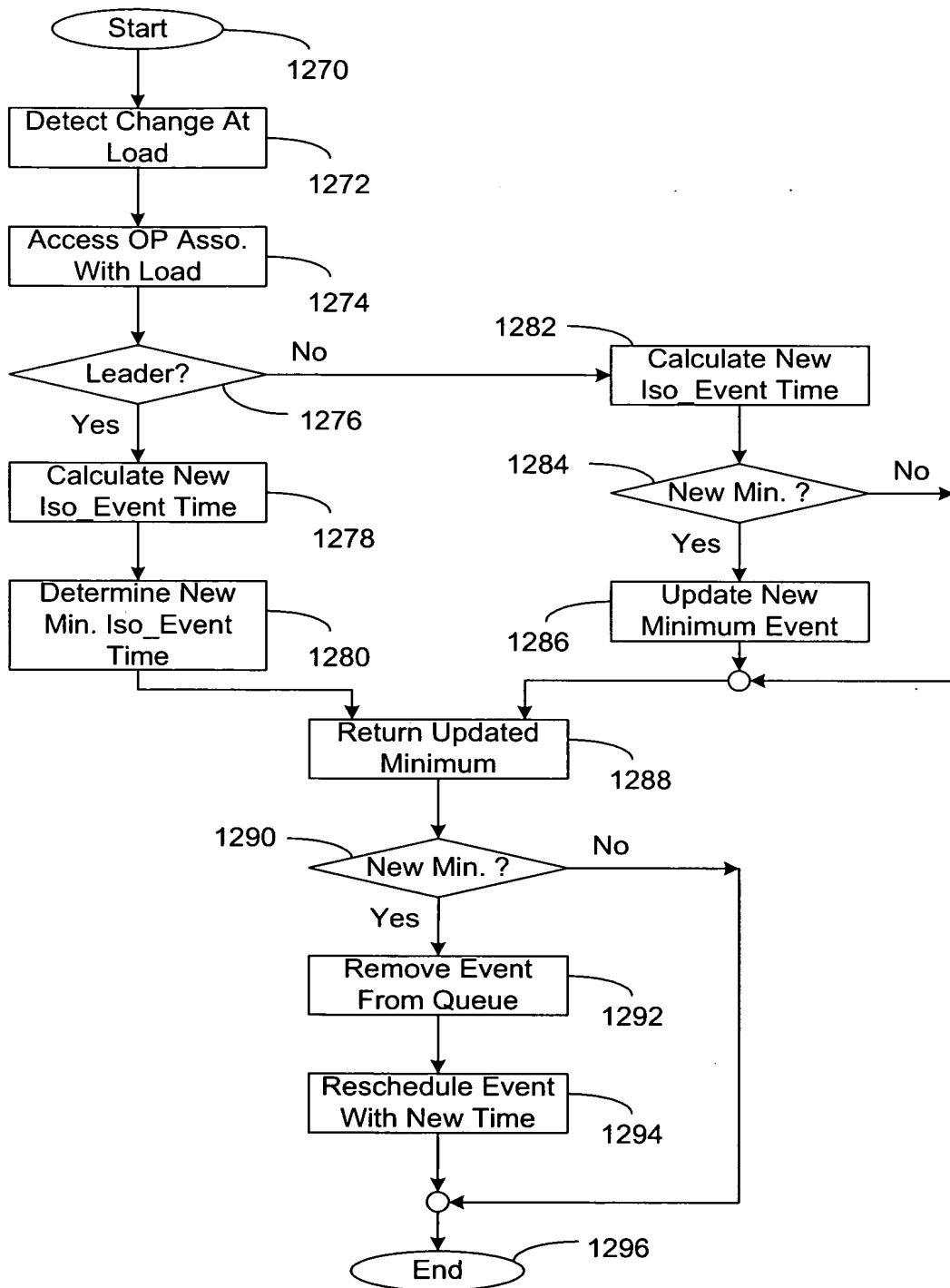


FIG. 12D

Event Diagram

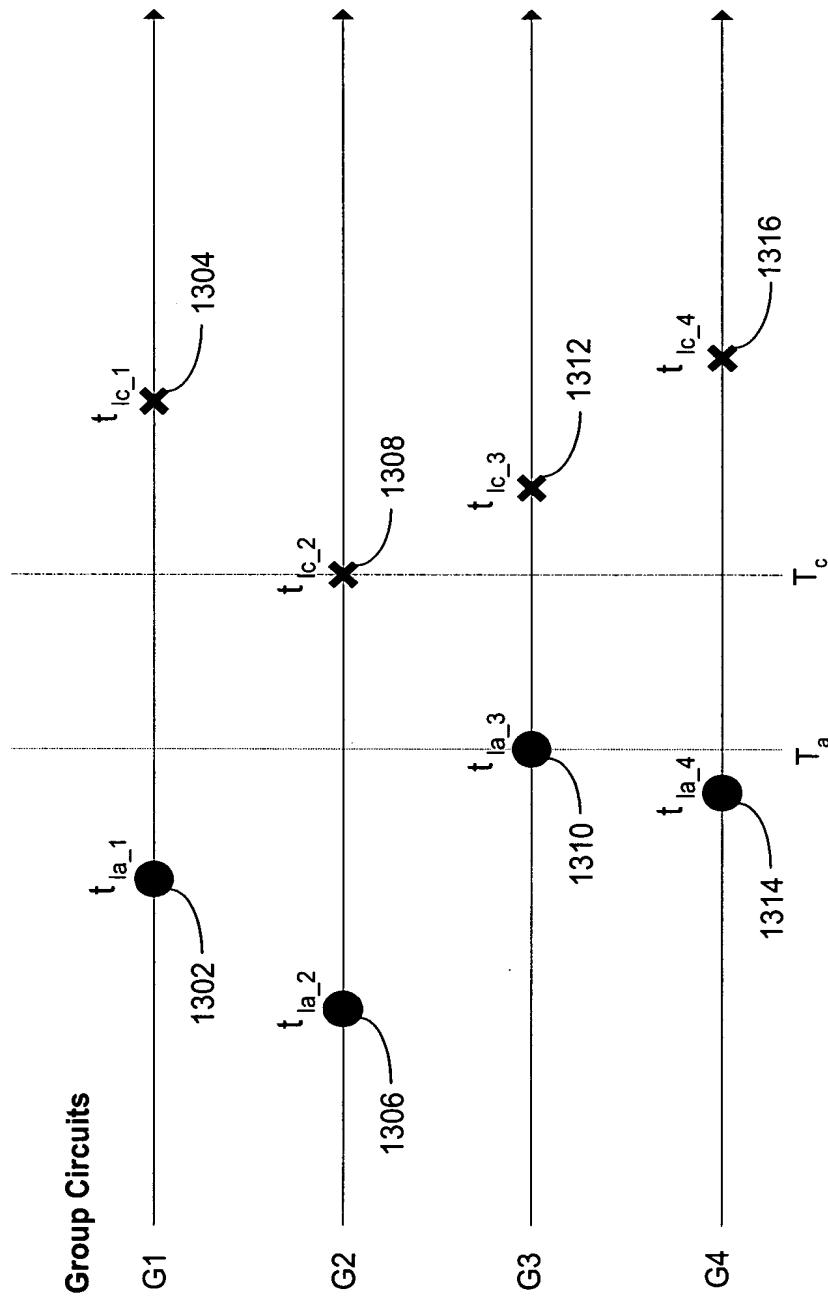


FIG. 13A

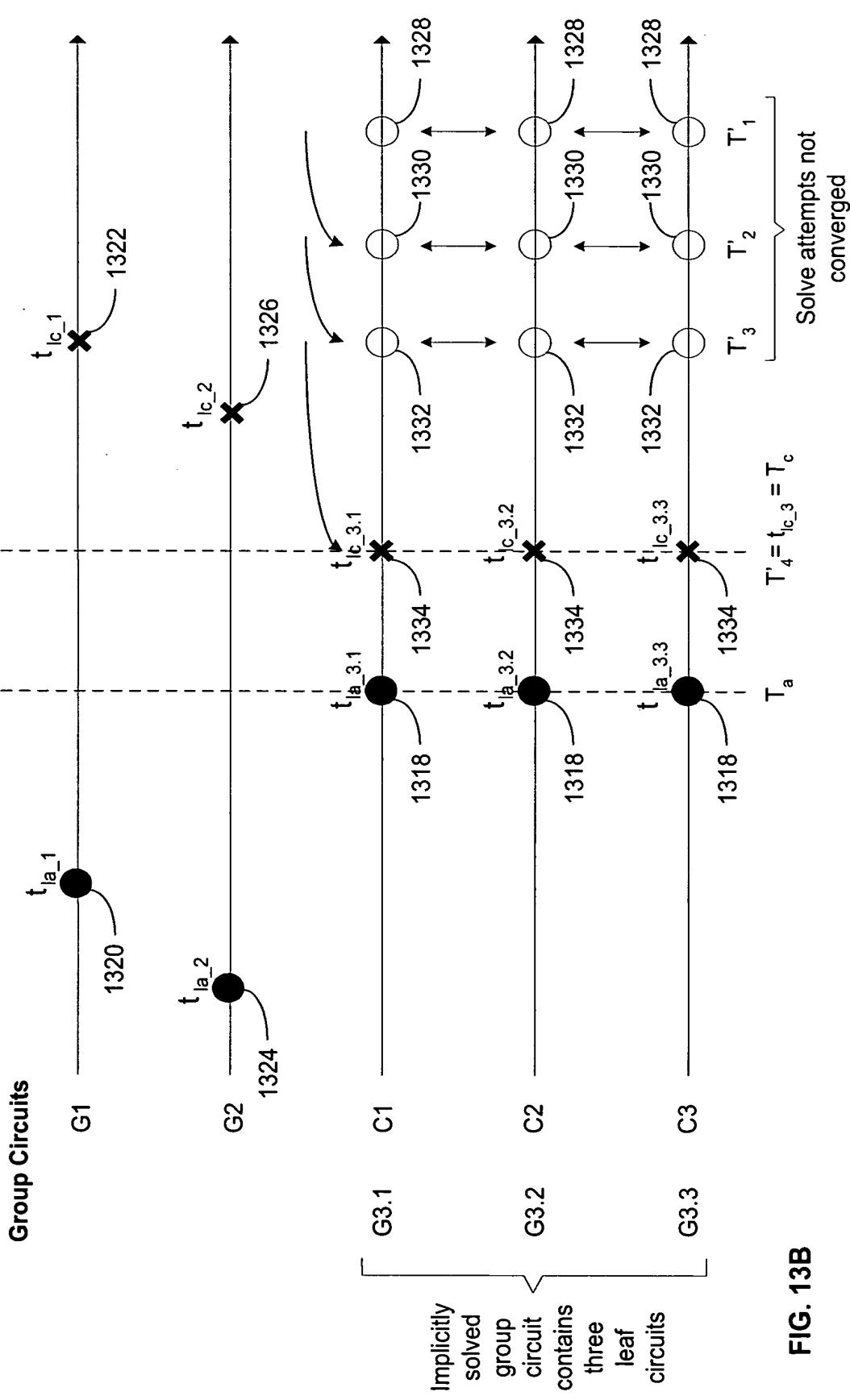


FIG. 13B

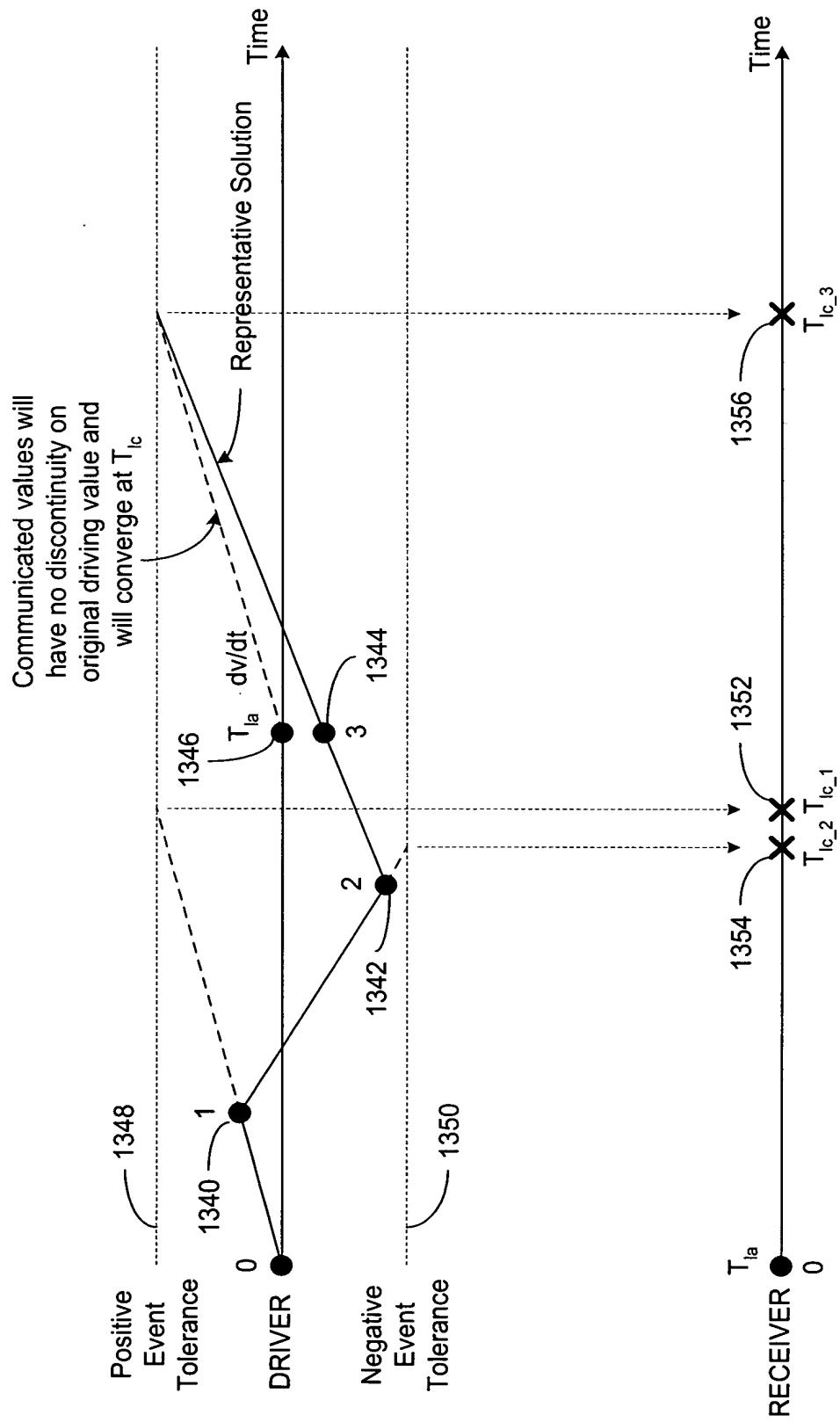


FIG. 13C

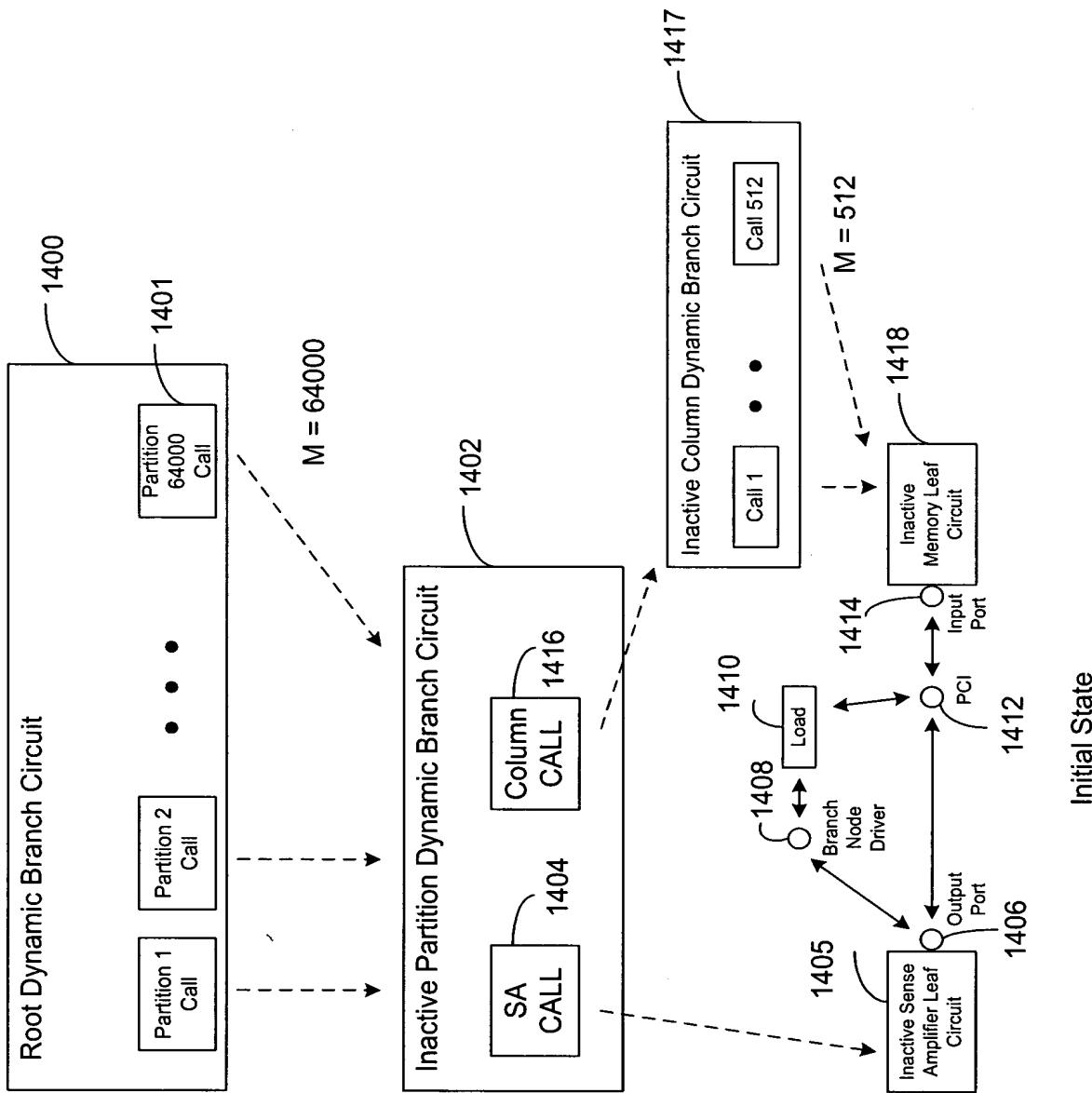
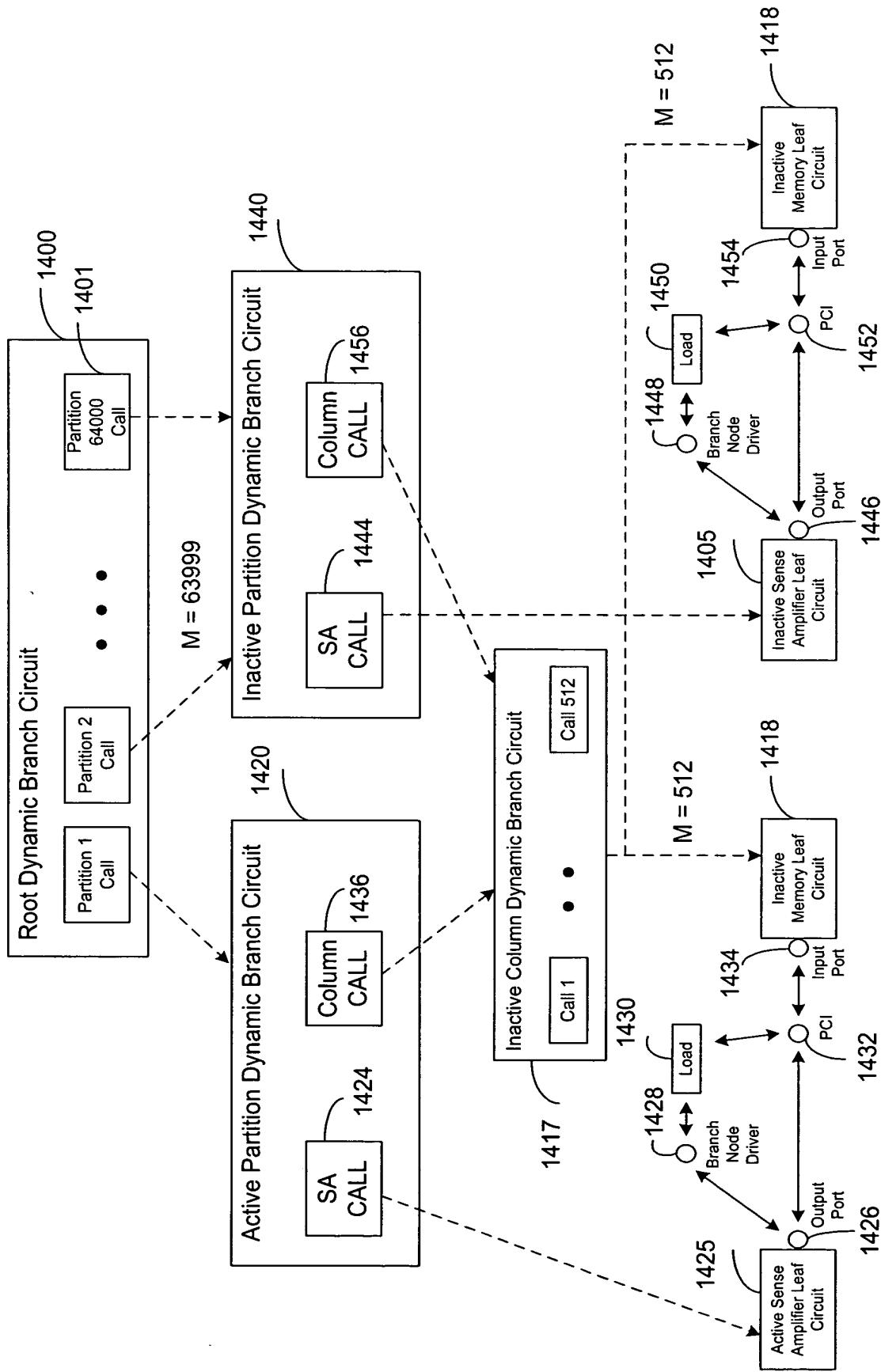


FIG. 14A



During Simulation When One Of The Sense Amplifiers Is Active
And The Column Driven By The Sense Amplifier Is Inactive

FIG. 14B

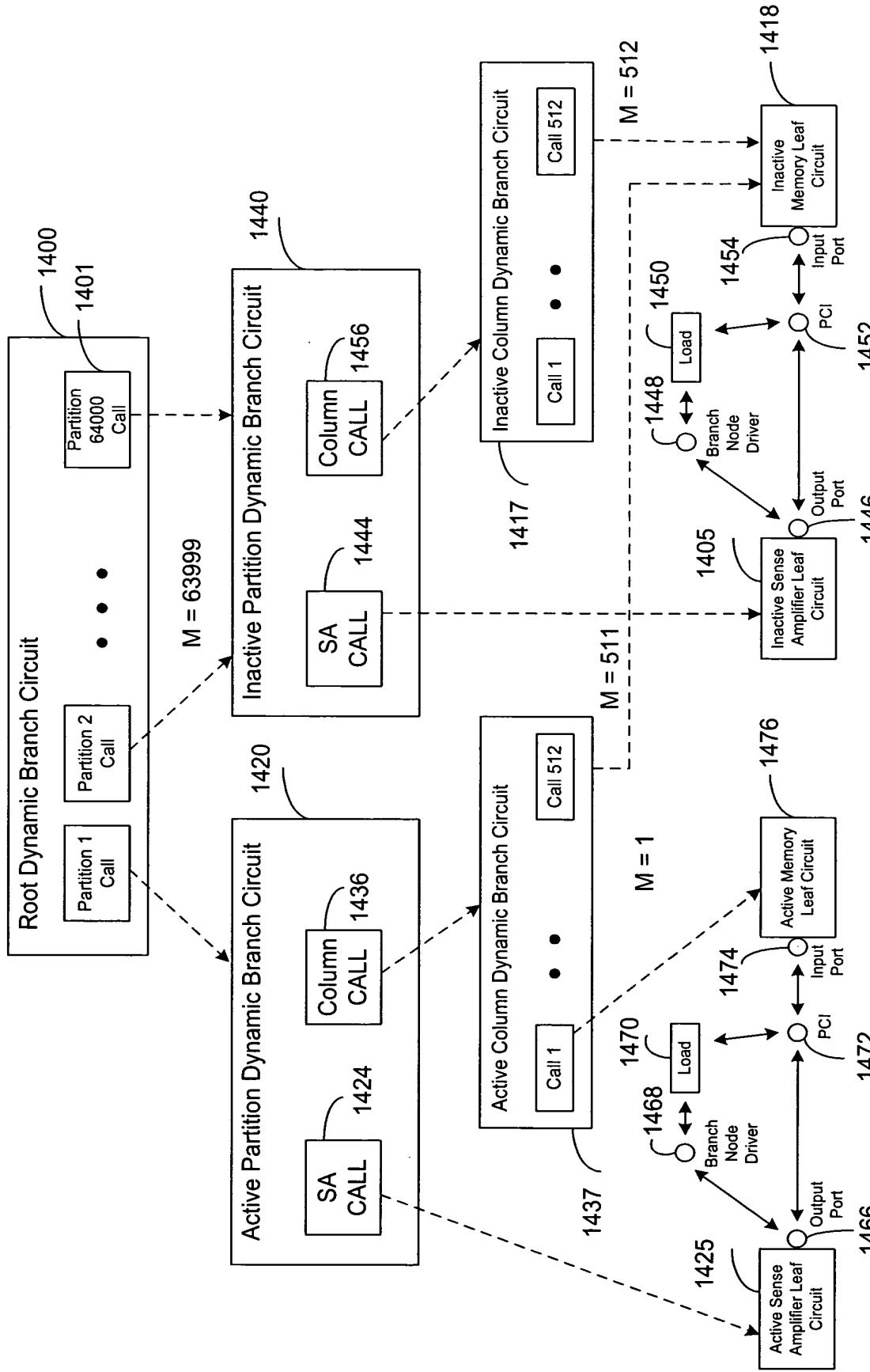


FIG. 14C

During Simulation When One Of The Memory Leaf Circuits Driven By The Corresponding Active Sense Amplifier Is Active